Lab 1 - Objective

In this lab, you will learn to design a custom logic component, 4-to-2 encoder, 2-to-4 decoder You don't have to simplify your design. We just need to see correct output on the timing simulator)

## Part 1. Custom Logic Component ( /1)

Construction of a combinational logic for the truth table below

|  |  |
| --- | --- |
| A B C (in) | F (out) |
| 000  001  010  011  100  101  110  111 | 0  1  1  0  0  1  0  1 |

## Part 2. Encoder Design ( /2)

Construction of a combinational logic for the encoder

|  |  |
| --- | --- |
| A B C D (in) | X Y (out) |
| 0 0 0 1  0 0 1 0  0 1 0 0  1 0 0 0 | 0 0  0 1  1 0  1 1 |

## Part 3. Decoder Desing ( /2)

Construction of a combinational logic for the decoder

|  |  |
| --- | --- |
| W Z (in) | P Q R S (out) |
| 0 0  0 1  1 0  1 1 | 0 0 0 1  0 0 1 0  0 1 0 0  1 0 0 0 |

Demo your simulation result to the TA to receive credit. Due date: Saturday 01/24/2015 4:00pm

You can show your results any time during the week on the TA hours.